IN THE CLAIMS

Please amend claim 26 as follows.

1-25. (Cancelled)

26. (Currently Amended) A semiconductor package comprising:

a substrate having opposing first and second surfaces and a rectangular through hole extending through the substrate between the first and second surfaces, said rectangular through hole having four sides;

a first conductive circuit pattern disposed on the first surface of the substrate, and a second conductive pattern disposed on the second surface of the substrate, wherein the first conductive circuit pattern includes at least bond fingers and lands, the second conductive pattern includes at least lands, and at least some of the first and second circuit patterns are electrically coupled through the substrate;

a first semiconductor chip having opposed active and inactive surfaces, wherein the first semiconductor chip is disposed within the through hole without contacting the substrate, and the active surface of the first semiconductor chip includes bond pads;

a second semiconductor chip having opposed active and inactive surfaces, wherein the second semiconductor chip is disposed within or over the through hole without contacting the substrate, and the active surface of the second semiconductor chip includes bond pads,

wherein the inactive surface of the second semiconductor chip faces and is mounted on the active surface of the first semiconductor chip so that the active surfaces of the first and second semiconductor chips are oriented in a same direction;

a plurality of first conductive wires, wherein each of the first conductive wires electrically connects a respective one of the bond pads of the first semiconductor chip to a respective one of the bond fingers of the first conductive circuit pattern;

a plurality of second conductive wires, wherein each of the second conductive wires electrically connects a respective one of the bond pads of the second semiconductor chip to a respective one of the bond fingers of the first conductive circuit pattern, at least some of said first and second conductive wires being electrically connected to bond fingers located adjacent a first side of the rectangular through hole, and at least some of said first and second conductive wires being electrically connected to bond fingers located adjacent a second side of the rectangular through hole, the first and second sides of the through hole being opposite one another; and

an encapsulant filling the through hole and contacting the first surface of the substrate, the bond fingers of the first conductive circuit pattern, the first semiconductor chip, the second semiconductor chip, and the first and second conductive wires,

wherein the inactive surface of the first semiconductor chip is exposed through the encapsulant in a common plane with the second surface of the substrate, and the lands of the first and second conductive circuit patterns are uncovered by the encapsulant.

27. (Previously Presented) The semiconductor package of claim 26, wherein the inactive surface of the second semiconductor chip has a smaller area than the active surface of the first semiconductor chip.

28. (Previously Presented) The semiconductor package of claim 26, wherein the first and second semiconductor chips are a same size.

29. (Previously Presented) The semiconductor package of claim 26, further comprising a plurality of conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the second conductive circuit pattern, and the active surfaces of the first and second semiconductor dies are oriented in a same direction as the first surface of the substrate.

30. (Previously Presented) The semiconductor package of claim 29, wherein the inactive surface of the second semiconductor chip has a smaller area than the active surface of the first semiconductor chip.

31. (Previously Presented) The semiconductor package of claim 29, wherein the first and second semiconductor chips are a same size.

32. (Previously Presented) The semiconductor package of claim 26, further comprising a plurality of conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first conductive circuit pattern, and the active surfaces of the first and second semiconductor dies are oriented in a same direction as the first surface of the substrate.

33. (Previously Presented) The semiconductor package of claim 32, wherein the inactive surface of the second

semiconductor chip has a smaller area than the active surface of the first semiconductor chip.

34. (Previously Presented) The semiconductor package of claim 32, wherein the first and second semiconductor chips are a same size.